## REMARKS

Claims 1-49 were originally filed in the present application. No claims were previously or are presently canceled or added. Thus, claims 1-49 remain pending in the present application. Reconsideration of this application in light of the above amendments and the following remarks is requested.

**Rejections under 35 U.S.C. §102(e)**

Claims 1, 5-7, 11-14, 38 and 44 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Application Publication No. 20040173815, having Yeo, et al., named as inventor ("Yeo '815"). However, rejections based on 35 U.S.C. §102(e) cannot be supported by Yeo '815 as applied to claims 1, 5-7, 11, 12-14, 38 and 44, for at least the following reasons.

Claim 1

Claim 1 recites:

> 1. A semiconductor device, comprising:
> an isolation region located in a substrate;
> an NMOS device located partially over a surface of the substrate; and
> a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface;
> wherein a first one of the NMOS and PMOS devices includes one of:
> first source/drain regions recessed within the surface; and
> first source/drain regions extending from the surface; and
> wherein a second one of the NMOS and PMOS devices includes one of:
> second source/drain regions recessed within the surface wherein the first source/drain regions extend from the surface;
> second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and
> second source/drain regions substantially coplanar with the surface.

The PTO provides in MPEP §2131 that "[t]o anticipate a claim, the reference must teach every element of the claim." Therefore, to support a rejection with respect to claim 1, Yeo '815 must contain all of the elements of claim 1. However, Yeo '815 does not disclose an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions recessed within the surface, and (2) first source/drain regions extending from the surface; and wherein a second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions recessed within the surface wherein the first source/drain regions extend from the surface; (2) second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and (3) second source/drain regions substantially coplanar with the surface.

For example, to support a rejection of claim 1, Yeo '815 must disclose an NMOS device and a PMOS device each located partially over a substrate surface, but Yeo '815 (for example, in Figs. 8A-8D and paragraph [0049], cited by the Examiner) does not explicitly disclose an NMOS device ***and*** a PMOS device ***each*** located partially over ***a*** substrate surface. That is, the portions of Yeo '815 cited by the Examiner only explicitly discloses a single MOS device.

In addition, to support a rejection of claim 1, Yeo '815 must also disclose that one of an NMOS device and a PMOS device includes first source/drain regions that are either recessed within or extending from the substrate surface, and that the other of the NMOS and PMOS devices includes second source/drain regions that are:

- recessed within the substrate surface if the first source/drain regions extend from the substrate surface;
- extending from the substrate surface if the first source/drain regions are recessed within the substrate surface; or
- substantially coplanar with the substrate surface.

Thus, to support a rejection of claim 1, Yeo '815 must disclose an NMOS device ***and*** a PMOS device ***each*** located partially over ***a*** substrate surface where:

- the NMOS device includes source/drain regions that are recessed within the substrate surface, and the PMOS device includes source/drain regions that are extending from the substrate surface;
- the PMOS device includes source/drain regions that are recessed within the substrate surface, and the NMOS device includes source/drain regions that are extending from the substrate surface;
- the NMOS device includes source/drain regions that are recessed within the substrate surface, and the PMOS device includes source/drain regions that are substantially coplanar with the substrate surface;
- the PMOS device includes source/drain regions that are recessed within the substrate surface, and the NMOS device includes source/drain regions that are substantially coplanar with the substrate surface;
- the NMOS device includes source/drain regions that are extending from the substrate surface, and the PMOS device includes source/drain regions that are substantially coplanar with the substrate surface; or
- the PMOS device includes source/drain regions that are extending from the substrate surface, and the NMOS device includes source/drain regions that are substantially coplanar with the substrate surface.

However, Yeo '815 fails to explicitly disclose any of these configurations. Consequently, rejections based on 35 U.S.C. §102(e) cannot be supported by Yeo '815 as applied to claim 1.

Claim 38

Claim 38 recites:

> 38. A semiconductor device, comprising:
> an isolation region located in a substrate;
> an NMOS device located partially over a surface of the substrate; and
> a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface;
> wherein a first one of the NMOS and PMOS devices includes one of:
>  first source/drain regions located at least partially within the substrate and comprising SiC; and
>  first source/drain regions located at least partially within the substrate and comprising SiGe; and
> wherein a second one of the NMOS and PMOS devices includes one of:
>  second source/drain regions located at least partially within the substrate and comprising SiC wherein the first source/drain regions comprise SiGe;
>  second source/drain regions located at least partially within the substrate and comprising SiGe wherein the first source/drain regions comprise SiC; and
>  second source/drain regions located at least partially within the substrate and substantially not comprising either of SiC and SiGe.

To support a rejection with respect to claim 38, Yeo '815 must contain all of the elements of claim 38. However, Yeo '815 does not disclose an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions located at least partially within the substrate and comprising SiC; and (2) first source/drain regions located at least partially within the substrate and comprising SiGe; and wherein a second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions located at least partially within the substrate and comprising SiC wherein the first source/drain regions comprise SiGe; (2) second source/drain regions located at least partially within the substrate and comprising SiGe wherein the first source/drain

regions comprise SiC; and (3) second source/drain regions located at least partially within the substrate and substantially not comprising either of SiC and SiGe.

For example, to support a rejection of claim 38, Yeo '815 must disclose an NMOS device and a PMOS device each located partially over a substrate surface and isolated from one another by an isolation region in the substrate, but Yeo '815 (for example, in Figs. 8A-8D and paragraph [0049], cited by the Examiner) does not explicitly disclose an NMOS device ***and*** a PMOS device ***each*** located partially over ***a*** substrate surface ***and***, consequently, an isolation region in the substrate isolating the NMOS device from the PMOS device. That is, the portions of Yeo '815 cited by the Examiner only explicitly disclose a single MOS device.

In addition, to support a rejection of claim 38, Yeo '815 must also disclose that one of the NMOS device and the PMOS device includes first source/drain regions that either comprise SiC or SiGe, and that the other of the NMOS device and the PMOS device includes second source/drain regions that comprise:

- SiC if the first source/drain regions comprise SiGe;
- SiGe if the first source/drain regions comprise SiC; or
- neither SiC nor SiGe.

Thus, to support a rejection of claim 38, Yeo '815 must disclose an NMOS device ***and*** a PMOS device ***each*** located partially over ***a*** substrate surface ***and*** isolated by an isolation region in the substrate where:

- the NMOS device includes source/drain regions that comprise SiC, and the PMOS device includes source/drain regions that comprise SiGe;
- the PMOS device includes source/drain regions that comprise SiC, and the NMOS device includes source/drain regions that comprise SiGe;
- the NMOS device includes source/drain regions that comprise SiC, and the PMOS device includes source/drain regions that comprise neither SiC nor SiGe;

- the PMOS device includes source/drain regions that comprise SiC, and the NMOS device includes source/drain regions that comprise neither SiC nor SiGe;
- the NMOS device includes source/drain regions that comprise SiGe, and the PMOS device includes source/drain regions that comprise neither SiC nor SiGe; or
- the PMOS device includes source/drain regions that comprise SiGe, and the NMOS device includes source/drain regions that comprise neither SiC nor SiGe.

However, Yeo '815 fails to explicitly disclose any of these configurations. Consequently, rejections based on 35 U.S.C. §102(e) cannot be supported by Yeo '815 as applied to claim 38.

Claim 44

Claim 44 recites:

> 44. A method of manufacturing a semiconductor device, comprising:
> forming an isolation region located in a substrate;
> forming an NMOS device located partially over a surface of the substrate; and
> forming a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface;
> wherein a first one of the NMOS and PMOS devices includes one of:
> first source/drain regions recessed within the surface; and
> first source/drain regions extending from the surface; and
> wherein a second one of the NMOS and PMOS devices includes one of:
> second source/drain regions recessed within the surface wherein the first source/drain regions extend from the surface;
> second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and
> second source/drain regions substantially coplanar with the surface.

To support a rejection with respect to claim 44, Yeo '815 must contain all of the elements of claim 44. However, Yeo '815 does not disclose forming an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions recessed within the surface, and (2) first source/drain regions extending from the surface; and wherein a second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions recessed within the surface wherein the first source/drain regions extend from the surface; (2) second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and (3) second source/drain regions substantially coplanar with the surface.

For example, to support a rejection of claim 44, Yeo '815 must disclose an NMOS device and a PMOS device each located partially over a substrate surface, but the portions of Yeo '815 cited by the Examiner do not explicitly disclose an NMOS device ***and*** a PMOS device ***each*** located partially over ***a*** substrate surface. That is, the cited portions of Yeo '815 only explicitly disclose a single MOS device.

In addition, to support a rejection of claim 44, Yeo '815 must also disclose that one of the NMOS device and the PMOS device includes first source/drain regions that are either recessed within or extending from the substrate surface, and that the other of the NMOS device and the PMOS device includes second source/drain regions that are:

- recessed within the substrate surface if the first source/drain regions extend from the substrate surface;
- extending from the substrate surface if the first source/drain regions are recessed within the substrate surface; or
- substantially coplanar with the substrate surface.

Thus, to support a rejection of claim 44, Yeo '815 must disclose an NMOS device ***and*** a PMOS device ***each*** located partially over ***a*** substrate surface where:

- the NMOS device includes source/drain regions that are recessed within the substrate surface, and the PMOS device includes source/drain regions that are extending from the substrate surface;
- the PMOS device includes source/drain regions that are recessed within the substrate surface, and the NMOS device includes source/drain regions that are extending from the substrate surface;
- the NMOS device includes source/drain regions that are recessed within the substrate surface, and the PMOS device includes source/drain regions that are substantially coplanar with the substrate surface;
- the PMOS device includes source/drain regions that are recessed within the substrate surface, and the NMOS device includes source/drain regions that are substantially coplanar with the substrate surface;
- the NMOS device includes source/drain regions that are extending from the substrate surface, and the PMOS device includes source/drain regions that are substantially coplanar with the substrate surface; or
- the PMOS device includes source/drain regions that are extending from the substrate surface, and the NMOS device includes source/drain regions that are substantially coplanar with the substrate surface.

However, Yeo '815 fails to explicitly disclose any of these configurations. Consequently, rejections based on 35 U.S.C. §102(e) cannot be supported by Yeo '815 as applied to claim 44.

**Rejections under 35 U.S.C. §103(a): Yeo '815 in view of Tao**

Claims 2, 16-20, 24-26, 40 and 45 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yeo '815 in view of U.S. Patent No. 6,524,938 to Tao, et al. ("Tao"). Applicants traverse these rejections on the grounds that Yeo '815 and Tao are defective in establishing a *prima facie* case of obviousness with respect to claims 1, 16, 38 and 44 and their respective dependent claims.

Claim 1

As the PTO recognizes in MPEP §2142:

> *The Examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness. If the Examiner does not produce a prima facie case, the applicant is under no obligation to submit evidence of nonobviousness.*

The Examiner cannot establish a *prima facie* case of obviousness based on the combination of Yeo '815 and Tao in connection with claim 1 since 35 U.S.C. §103(a) provides that:

> *[a] patent may not be obtained ... if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains ... (emphasis added)*

Thus, when evaluating a claim for determining obviousness, all limitations of the claim must be evaluated. However, as described above, Yeo '815 fails to teach any of the configurations recited in claim 1. Moreover, Tao fails to cure this shortcoming, because Tao also fails to teach an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; and (2) a first gate interposing the first source/drain regions and having a first gate height over the surface; and wherein a second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; and (2) a second gate interposing the second source/drain regions and having a second gate height over the surface, wherein the first and second gate heights are substantially different, where the substantial difference between the first and second gate heights at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first

and second source/drain regions, respectively. That is, Tao fails to teach any of the configurations recited in claim 1 in the manner described above with respect to Yeo '815.

Therefore, it is impossible to render obvious the subject matter of claim 1 based on the combination of Yeo '815 and Tao, and the above explicit terms of the statute cannot be met. As a result, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 1, and a rejection under 35 U.S.C. §103(a) is not applicable to claim 1 or its dependent claims.

There is still another compelling, and mutually exclusive, reason why the combination of Yeo '815 and Tao cannot be combined and applied to reject claim 1 under 35 U.S.C. §103(a).

The PTO also provides in MPEP §2142:

> *[T]he Examiner must step backward in time and into the shoes worn by the hypothetical "person of ordinary skill in the art" when the invention was unknown and just before it was made. In view of all factual information, the Examiner must then make a determination whether the claimed invention "as a whole" would have been obvious at that time to that person. ...[I]mpermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art.*

Here, the combination of Yeo '815 and Tao does not teach, or even suggest, the desirability of combination since neither Yeo '815 nor Tao teach or suggest providing an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; and (2) a first gate interposing the first source/drain regions and having a first gate height over the surface; and wherein a second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; and (2) a second gate interposing the second source/drain regions and having a second gate height over the surface, wherein the first and second gate heights are substantially different, where the substantial difference between the first and second gate heights at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first and second source/drain regions,

respectively. That is, neither Yeo '815 nor Tao teaches any of the configurations recited in claim 1 in the manner described above.

Thus, neither Yeo '815 nor Tao provide any incentive or motivation supporting the desirability of combination. Therefore, there is simply no basis in the art for combining Yeo '815 and Tao to support a 35 U.S.C. §103(a) rejection of claim 1. Consequently, for this mutually exclusive reason, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 1 and its dependent claims. Accordingly, the rejection of claim 2 under 35 U.S.C. §103(a) is not applicable.

Claim 16

Claim 16 recites:

> 16. A semiconductor device, comprising:
> an isolation region located in a substrate;
> an NMOS device located partially over a surface of the substrate; and
> a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface;
> wherein a first one of the NMOS and PMOS devices includes:
> first source/drain regions located at least partially in the substrate; and
> a first gate interposing the first source/drain regions and having a first gate height over the surface; and
> wherein a second one of the NMOS and PMOS devices includes:
> second source/drain regions located at least partially in the substrate; and
> a second gate interposing the second source/drain regions and having a second gate height over the surface, wherein the first and second gate heights are substantially different, where the substantial difference between the first and second gate heights at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first and second source/drain regions, respectively.

Yeo '815 and Tao, whether alone or in combination, do not teach an NMOS device and a PMOS device each located partially over a substrate surface and isolated by an isolation region located in the substrate between the NMOS and PMOS devices, wherein a first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; and (2) a first gate interposing the first source/drain regions and having a first gate height over the surface; and wherein a second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; and (2) a second gate interposing the second source/drain regions and having a second gate height over the surface, wherein the first and second gate heights are substantially different, where the substantial difference between the first and second gate heights at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first and second source/drain regions, respectively.

For example, to support a rejection of claim 16, either Yeo '815 or Tao must teach an NMOS device and a PMOS device each located partially over a substrate surface and isolated by an isolation region located in the substrate between the NMOS and PMOS devices, but neither Yeo '815 nor Tao teach an NMOS device ***and*** a PMOS device ***each*** located partially over ***a*** substrate surface ***and*** isolated by an isolation region in the substrate.

In addition, to support a rejection of claim 16, either Yeo '815 or Tao must also teach that the NMOS and PMOS devices includes gates of substantially different heights over the substrate surface, where the substantial difference between the gate heights at least indirectly causes a substantial difference in magnitudes of stresses in source/drain regions of the NMOS and PMOS devices. However, neither Yeo '815 nor Tao teaches such a configuration. That is, neither Yeo '815 nor Tao teach NMOS and PMOS devices of a common substrate yet having source/drain regions with different magnitudes of stresses. Consequently, rejections based on 35 U.S.C. §103(a) cannot be supported by the combination of Yeo '815 and Tao as applied to claim 16.

Therefore, it is impossible to render obvious the subject matter of claim 16 based on the combination of Yeo '815 and Tao, and the above explicit terms of the statute cannot be met. As a result, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot

be met with respect to claim 16, and a rejection under 35 U.S.C. §103(a) is not applicable to claim 16 and its dependent claims.

There is still another compelling, and mutually exclusive, reason why the combination of Yeo '815 and Tao cannot be applied to reject claim 16 under 35 U.S.C. §103(a). Here, the combination of Yeo '815 and Tao does not teach, or even suggest, the desirability of combination since neither teach or suggest providing an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; and (2) a first gate interposing the first source/drain regions and having a first gate height over the surface; and wherein a second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; and (2) a second gate interposing the second source/drain regions and having a second gate height over the surface, wherein the first and second gate heights are substantially different, where the substantial difference between the first and second gate heights at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first and second source/drain regions, respectively.

Thus, neither Yeo '815 nor Tao provide any incentive or motivation supporting the desirability of combination. Therefore, there is simply no basis in the art for combining Yeo '815 and Tao to support a 35 U.S.C. §103(a) rejection of claim 16. Consequently, for this mutually exclusive reason, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 16, and the rejection under 35 U.S.C. §103(a) is not applicable to claim 16 or its dependent claims.

The Examiner also alleges that claim 16 includes functional limitations which carry no patentable. However, the PTO provides in MPEP §2173.05(g):

> *There is nothing inherently wrong with defining some part of an invention in functional terms. Functional language does not, in and of itself, render a claim improper. ... A functional limitation must be evaluated and considered, just like any other limitation of the claim, for what it fairly conveys to a person of ordinary skill in the pertinent art in the context in which it is used. A functional limitation is often used in association with an element,*

*ingredient, or step of a process to define a particular capability or purpose that is served by the recited element, ingredient or step.*

In the present context, the claimed difference between gate heights as at least indirectly causing a substantial difference in magnitudes of stresses in respective source/drain regions defines structural attributes of interrelated components of the claimed configuration. As also provided in MPEP §2173.05(g), such functional limitations that define structural attributes of interrelated components have been held to be patentably distinguishable limitations. Therefore, the Examiner is in incorrect in alleging that no patentable weight should be given to the claimed difference between gate heights which at least indirectly causes a substantial difference in magnitudes of stresses in respective source/drain regions.

Claim 38

As described above, Yeo '815 fails to teach any of the configurations recited in claim 38. Moreover, Tao fails to cure this shortcoming, because Tao also fails to teach an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions located at least partially within the substrate and comprising SiC; and (2) first source/drain regions located at least partially within the substrate and comprising SiGe; and wherein a second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions located at least partially within the substrate and comprising SiC wherein the first source/drain regions comprise SiGe; (2) second source/drain regions located at least partially within the substrate and comprising SiGe wherein the first source/drain regions comprise SiC; and (3) second source/drain regions located at least partially within the substrate and substantially not comprising either of SiC and SiGe.

Therefore, it is impossible to render obvious the subject matter of claim 38 based on the combination of Yeo '815 and Tao, and the above explicit terms of the statute cannot be met. As a result, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot

be met with respect to claim 38, and a rejection under 35 U.S.C. §103(a) is not applicable to claim 38 and its dependent claims.

There is still another compelling, and mutually exclusive, reason why the combination of Yeo '815 and Tao cannot be applied to reject claim 38 under 35 U.S.C. §103(a). Here, the combination of Yeo '815 and Tao does not teach, or even suggest, the desirability of combination since neither teach or suggest an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions located at least partially within the substrate and comprising SiC; and (2) first source/drain regions located at least partially within the substrate and comprising SiGe; and wherein a second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions located at least partially within the substrate and comprising SiC wherein the first source/drain regions comprise SiGe; (2) second source/drain regions located at least partially within the substrate and comprising SiGe wherein the first source/drain regions comprise SiC; and (3) second source/drain regions located at least partially within the substrate and substantially not comprising either of SiC and SiGe.

Thus, neither Yeo '815 nor Tao provide any incentive or motivation supporting the desirability of combination. Therefore, there is simply no basis in the art for combining Yeo '815 and Tao to support a 35 U.S.C. §103(a) rejection of claim 38. Therefore, for this mutually exclusive reason, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 38 and its dependent claims. Consequently, the rejection of claim 40 under 35 U.S.C. §103(a) is not applicable.

Claim 44

As described above, Yeo '815 fails to teach any of the configurations recited in claim 44. Moreover, Tao fails to cure this shortcoming, because Tao also fails to teach forming an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions recessed within the surface, and (2) first source/drain regions extending from the surface; and wherein a second one

of the NMOS and PMOS devices includes one of: (1) second source/drain regions recessed within the surface wherein the first source/drain regions extend from the surface; (2) second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and (3) second source/drain regions substantially coplanar with the surface.

Therefore, it is impossible to render obvious the subject matter of claim 44 based on the combination of Yeo '815 and Tao, and the above explicit terms of the statute cannot be met. As a result, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 44, and a rejection under 35 U.S.C. §103(a) is not applicable to claim 44 and its dependent claims.

There is still another compelling, and mutually exclusive, reason why the combination of Yeo '815 and Tao cannot be applied to reject claim 44 under 35 U.S.C. §103(a). Here, the combination of Yeo '815 and Tao does not teach, or even suggest, the desirability of combination since neither teach or suggest forming an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions recessed within the surface, and (2) first source/drain regions extending from the surface; and wherein a second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions recessed within the surface wherein the first source/drain regions extend from the surface; (2) second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and (3) second source/drain regions substantially coplanar with the surface.

Thus, neither Yeo '815 nor Tao provide any incentive or motivation supporting the desirability of combination. Therefore, there is simply no basis in the art for combining Yeo '815 and Tao to support a 35 U.S.C. §103(a) rejection of claim 44. Therefore, for this mutually exclusive reason, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 44 and its dependent claims. Consequently, the rejection of claim 45 under 35 U.S.C. §103(a) is not applicable.

**Rejection under 35 U.S.C. §103(a): Yeo '815 in view of Tao and Shimizu**

Claim 27 was rejected under 35 U.S.C. §103(a) as being unpatentable over Yeo '815 in view of Tao and further in view of Shimizu, et al., "Local Mechanical Stress Control," IEDM 2001, pp. 433-436 ("Shimizu"). Applicants traverse this rejection on the grounds that Yeo '815, Tao and Shimizu are defective in establishing a *prima facie* case of obviousness with respect to claim 16 and its dependent claims.

As described above, the combination of Yeo '815 and Tao fails to support a *prima facie* case of obviousness of claim 16 and its dependent claims. Moreover, Shimizu fails to correct this shortcoming because Shimizu also fails to teach an NMOS device and a PMOS device each located partially over a substrate surface and isolated by an isolation region located in the substrate between the NMOS and PMOS devices, wherein a first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; and (2) a first gate interposing the first source/drain regions and having a first gate height over the surface; and wherein a second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; and (2) a second gate interposing the second source/drain regions and having a second gate height over the surface, wherein the first and second gate heights are substantially different, where the substantial difference between the first and second gate heights at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first and second source/drain regions, respectively.

Therefore, it is impossible to render obvious the subject matter of claim 16 based on the combination of Yeo '815, Tao and Shimizu, and the above explicit terms of the statute cannot be met. As a result, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 16 and its dependent claims. Consequently, a rejection of claim 27 under 35 U.S.C. §103(a) is not applicable.

There is still another compelling, and mutually exclusive, reason why the combination of Yeo '815, Tao and Shimizu cannot be applied to reject claim 16 or its dependent claims under 35 U.S.C. §103(a). Here, the combination of Yeo '815, Tao and Shimizu does not teach, or even suggest, the desirability of combination since neither Yeo '815, Tao nor Shimizu teach or suggest

providing an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; and (2) a first gate interposing the first source/drain regions and having a first gate height over the surface; and wherein a second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; and (2) a second gate interposing the second source/drain regions and having a second gate height over the surface, wherein the first and second gate heights are substantially different, where the substantial difference between the first and second gate heights at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first and second source/drain regions, respectively.

Thus, neither Yeo '815, Tao nor Shimizu provide any incentive or motivation supporting the desirability of combination. Therefore, there is simply no basis in the art for combining Yeo '815, Tao and Shimizu to support a 35 U.S.C. §103(a) rejection of claim 16 and its dependent claims. Therefore, for this mutually exclusive reason, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 16 and its dependent claims. Consequently, the rejection of claim 27 under 35 U.S.C. §103(a) is not applicable.

**Rejection under 35 U.S.C. §103(a): Yeo '815 in view of Tao, Shimizu and Yeo '646**

Claims 21 and 22 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yeo '815 in view of Tao and Shimizu and further in view of U.S. Patent Application Publication No. 20040195646, having Yeo, et al., named as inventor ("Yeo '646"). Applicants traverse these rejections on the grounds that Yeo '815, Tao, Shimizu and Yeo '646 are defective in establishing a *prima facie* case of obviousness with respect to claim 16 and its dependent claims.

As described above, the combination of Yeo '815, Tao and Shimizu fails to support a *prima facie* case of obviousness of claim 16 and its dependent claims. Moreover, Yeo '646 fails to correct this shortcoming because Yeo '646 also fails to teach an NMOS device and a PMOS device each located partially over a substrate surface and isolated by an isolation region located

in the substrate between the NMOS and PMOS devices, wherein a first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; and (2) a first gate interposing the first source/drain regions and having a first gate height over the surface; and wherein a second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; and (2) a second gate interposing the second source/drain regions and having a second gate height over the surface, wherein the first and second gate heights are substantially different, where the substantial difference between the first and second gate heights at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first and second source/drain regions, respectively.

Therefore, it is impossible to render obvious the subject matter of claim 16 based on the combination of Yeo '815, Tao, Shimizu and Yeo '646, and the above explicit terms of the statute cannot be met. As a result, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 16 and its dependent claims. Consequently, the rejection of claims 21 and 22 under 35 U.S.C. §103(a) is not applicable.

There is still another compelling, and mutually exclusive, reason why the combination of Yeo '815, Tao, Shimizu and Yeo '646 cannot be applied to reject claim 16 or its dependent claims under 35 U.S.C. §103(a). Here, the combination of Yeo '815, Tao, Shimizu and Yeo '646 does not teach, or even suggest, the desirability of combination since neither Yeo '815, Tao, Shimizu nor Yeo '646 teach or suggest providing an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; and (2) a first gate interposing the first source/drain regions and having a first gate height over the surface; and wherein a second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; and (2) a second gate interposing the second source/drain regions and having a second gate height over the surface, wherein the first and second gate heights are substantially different, where the substantial difference between the first and second gate heights at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first and second source/drain regions, respectively.

Thus, neither Yeo '815, Tao, Shimizu nor Yeo '646 provide any incentive or motivation supporting the desirability of combination. Therefore, there is simply no basis in the art for combining Yeo '815, Tao, Shimizu and Yeo '646 to support a 35 U.S.C. §103(a) rejection of claim 16 and its dependent claims. Therefore, for this mutually exclusive reason, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 16 and its dependent claims. Consequently, the rejection of claims 21 and 22 under 35 U.S.C. §103(a) is not applicable.

**Rejection under 35 U.S.C. §103(a): Yeo '815 in view of Tao and Baba**

Claim 23 was rejected under 35 U.S.C. §103(a) as being unpatentable over Yeo '815 in view of Tao and further in view of U.S. Patent No. 6,774,409 to Baba, et al. ("Baba"). Applicants traverse this rejection on the grounds that Yeo '815, Tao and Baba are defective in establishing a *prima facie* case of obviousness with respect to claim 16 and its dependent claims.

As described above, the combination of Yeo '815 and Tao fails to support a *prima facie* case of obviousness of claim 16 and its dependent claims. Moreover, Baba fails to correct this shortcoming because Baba also fails to teach an NMOS device and a PMOS device each located partially over a substrate surface and isolated by an isolation region located in the substrate between the NMOS and PMOS devices, wherein a first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; and (2) a first gate interposing the first source/drain regions and having a first gate height over the surface; and wherein a second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; and (2) a second gate interposing the second source/drain regions and having a second gate height over the surface, wherein the first and second gate heights are substantially different, where the substantial difference between the first and second gate heights at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first and second source/drain regions, respectively.

Therefore, it is impossible to render obvious the subject matter of claim 16 based on the combination of Yeo '815, Tao and Baba, and the above explicit terms of the statute cannot be

met. As a result, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 16 and its dependent claims. Consequently, a rejection of claim 23 under 35 U.S.C. §103(a) is not applicable.

There is still another compelling, and mutually exclusive, reason why the combination of Yeo '815, Tao and Baba cannot be applied to reject claim 16 or its dependent claims under 35 U.S.C. §103(a). Here, the combination of Yeo '815, Tao and Baba does not teach, or even suggest, the desirability of combination since neither Yeo '815, Tao nor Baba teach or suggest providing an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; and (2) a first gate interposing the first source/drain regions and having a first gate height over the surface; and wherein a second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; and (2) a second gate interposing the second source/drain regions and having a second gate height over the surface, wherein the first and second gate heights are substantially different, where the substantial difference between the first and second gate heights at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first and second source/drain regions, respectively.

Thus, neither Yeo '815, Tao nor Baba provide any incentive or motivation supporting the desirability of combination. Therefore, there is simply no basis in the art for combining Yeo '815, Tao and Baba to support a 35 U.S.C. §103(a) rejection of claim 16 and its dependent claims. Therefore, for this mutually exclusive reason, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 16 and its dependent claims. Consequently, the rejection of claim 23 under 35 U.S.C. §103(a) is not applicable.

**Rejections under 35 U.S.C. §103(a): Yeo '815**

Claims 3, 4, 28-31, 36, 41, 42 and 46 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yeo '815. Applicants traverse these rejections on the grounds that Yeo '815 is

defective in establishing a *prima facie* case of obviousness with respect to independent claims 1, 28, 38 and 44 and their dependent claims.

Claim 1

As described above, Yeo '815 fails to teach an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions recessed within the surface, and (2) first source/drain regions extending from the surface; and wherein a second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions recessed within the surface wherein the first source/drain regions extend from the surface; (2) second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and (3) second source/drain regions substantially coplanar with the surface.

Therefore, it is impossible to render obvious the subject matter of claim 1 based on Yeo '815, and the above explicit terms of the statute cannot be met. As a result, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 1 and its dependent claims. Consequently, a rejection of claims 3 and 4 under 35 U.S.C. §103(a) is not applicable.

Moreover, Yeo '815 fails to provide any incentive or motivation for the modification suggested by the Examiner to arrive at the recitation of claim 1. Therefore, there is simply no basis in the art of record for modifying Yeo '815 as suggested by the Examiner to support a 35 U.S.C. §103(a) rejection of claim 1 and its dependent claims. Therefore, for this mutually exclusive reason, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 1 and its dependent claims. Consequently, the rejection of claims 3 and 4 under 35 U.S.C. §103(a) is not applicable.

Claim 28

Claim 28 recites:

> 28. A semiconductor device, comprising:
> an isolation region located in a substrate;
> an NMOS device located partially over a surface of the substrate; and
> a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface;
> wherein a first one of the NMOS and PMOS devices includes:
> first source/drain regions located at least partially in the substrate;
> a first gate interposing the first source/drain regions; and
> first spacers on opposing sides of the first gate and each extending from the first gate to a first width; and
> wherein a second one of the NMOS and PMOS devices includes:
> second source/drain regions located at least partially in the substrate;
> a second gate interposing the second source/drain regions; and
> second spacers on opposing sides of the second gate and each extending from the second gate to a second width, wherein the first and second widths are substantially different, where the substantial difference between the first and second widths at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first and second source/drain regions, respectively.

Yeo '815 does not teach an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; (2) a first gate interposing the first source/drain regions; and (3) first spacers on opposing sides of the first gate and each extending from the first gate to a first width; and wherein a second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; (2) a second gate interposing the second source/drain regions; and (3) second spacers on opposing sides of the second gate and each extending from the second gate to a second width, wherein the first and second widths are substantially different, where the substantial difference between the first and

second widths at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first and second source/drain regions, respectively.

For example, to support a rejection of claim 28, Yeo '815 must teach an NMOS device and a PMOS device each located partially over a substrate surface and isolated by an isolation region located in the substrate between the NMOS and PMOS devices, but Yeo '815 does not teach an NMOS device ***and*** a PMOS device ***each*** located partially over ***a*** substrate surface ***and*** isolated by an isolation region in the substrate.

In addition, to support a rejection of claim 28, Yeo '815 must also teach that the NMOS and PMOS devices includes spacers extending from respective spacers to substantially different widths, where the substantial difference between the spacer widths at least indirectly causes a substantial difference in magnitudes of stresses in source/drain regions of the NMOS and PMOS devices. However, Yeo '815 fails to teach such a configuration. Consequently, rejections based on 35 U.S.C. §103(a) cannot be supported by Yeo '815 as applied to claim 28.

Therefore, it is impossible to render obvious the subject matter of claim 28 based on Yeo '815, and the above explicit terms of the statute cannot be met. As a result, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 28, and a rejection under 35 U.S.C. §103(a) is not applicable.

Moreover, Yeo '815 fails to provide any incentive or motivation for the modification suggested by the Examiner to arrive at the recitation of claim 28. Therefore, there is simply no basis in the art of record for modifying Yeo '815 as suggested by the Examiner to support a 35 U.S.C. §103(a) rejection of claim 28 and its dependent claims. Therefore, for this mutually exclusive reason, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 28 and its dependent claims. Consequently, the rejection of claims 28-31 and 36 under 35 U.S.C. §103(a) is not applicable.

The Examiner also alleges that claim 28 includes functional limitations which carry no patentable weight. However, the PTO provides in MPEP §2173.05(g):

> *There is nothing inherently wrong with defining some part of an invention in functional terms. Functional language does not, in*

> *and of itself, render a claim improper. ... A functional limitation must be evaluated and considered, just like any other limitation of the claim, for what it fairly conveys to a person of ordinary skill in the pertinent art in the context in which it is used. A functional limitation is often used in association with an element, ingredient, or step of a process to define a particular capability or purpose that is served by the recited element, ingredient or step.*

In the present context, the claimed difference between spacer widths as at least indirectly causing a substantial difference in magnitudes of stresses in respective source/drain regions defines structural attributes of interrelated components of the claimed configuration. As also provided in MPEP §2173.05(g), such functional limitations which define structural attributes of interrelated components have been held to be patentably distinguishable limitations. Therefore, the Examiner is in incorrect in alleging that no patentable weight should be given to the claimed difference between spacer widths which at least indirectly causes a substantial difference in magnitudes of stresses in respective source/drain regions.

Claim 38

As described above, Yeo '815 fails to teach any of the configurations recited in claim 38. Thus, for at least this reason, Yeo '815 fails to support a *prima facie* case of obviousness of claim 38 and its dependent claims 41 and 42.

Moreover, Yeo '815 fails to provide any incentive or motivation for the modification suggested by the Examiner to arrive at the recitation of claim 38. Therefore, there is simply no basis in the art of record for modifying Yeo '815 to support a 35 U.S.C. §103(a) rejection of claim 38 and its dependent claims. Therefore, for this mutually exclusive reason, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 38 and its dependent claims. Consequently, the rejection of claims 41 and 42 under 35 U.S.C. §103(a) is not applicable.

Claim 44

As described above, Yeo '815 fails to teach any of the configurations recited in claim 44. Thus, for at least this reason, Yeo '815 fails to support a *prima facie* case of obviousness of claim 44 and its dependent claim 46.

Moreover, Yeo '815 fails to provide any incentive or motivation for the modification suggested by the Examiner to arrive at the recitation of claim 44 or its dependent claims. Therefore, there is simply no basis in the art of record for modifying Yeo '815 to support a 35 U.S.C. §103(a) rejection of claim 44 and its dependent claims. Therefore, for this mutually exclusive reason, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 44 and its dependent claims. Consequently, the rejection of claim 46 under 35 U.S.C. §103(a) is not applicable.

**Rejections under 35 U.S.C. §103(a): Yeo '815 in view of Shimizu**

Claims 15, 37 and 43 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yeo '815 in view of Shimizu. Applicants traverse these rejections on the grounds that the combination of Yeo '815 and Shimizu is defective in establishing a *prima facie* case of obviousness with respect to independent claims 1, 28 and 38 and their dependent claims.

Claim 1

As described above, Yeo '815 fails to teach any of the configurations recited in claim 1. Moreover, Shimizu fails to cure this shortcoming, because Shimizu also fails to teach an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; and (2) a first gate interposing the first source/drain regions and having a first gate height over the surface; and wherein a second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; and (2) a second gate interposing the second source/drain regions and having a second gate height over the surface, wherein the first and second gate heights are substantially different, where the substantial

difference between the first and second gate heights at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first and second source/drain regions, respectively. That is, Shimizu fails to teach any of the configurations recited in claim 1 in the manner described above with respect to Yeo '815.

Therefore, it is impossible to render obvious the subject matter of claim 1 based on the combination of Yeo '815 and Shimizu, and the above explicit terms of the statute cannot be met. As a result, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 1, and a rejection under 35 U.S.C. §103(a) is not applicable to claim 1 or its dependent claim 15.

Another compelling and mutually exclusive reason why the combination of Yeo '815 and Shimizu cannot be combined and applied to reject claim 1 under 35 U.S.C. §103(a) is that the combination of Yeo '815 and Shimizu does not teach, or even suggest, the desirability of combination since neither Yeo '815 nor Shimizu teach or suggest providing an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; and (2) a first gate interposing the first source/drain regions and having a first gate height over the surface; and wherein a second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; and (2) a second gate interposing the second source/drain regions and having a second gate height over the surface, wherein the first and second gate heights are substantially different, where the substantial difference between the first and second gate heights at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first and second source/drain regions, respectively. That is, neither Yeo '815 nor Shimizu teach any of the configurations recited in claim 1 in the manner described above.

Thus, neither Yeo '815 nor Shimizu provide any incentive or motivation supporting the desirability of combination. Therefore, there is simply no basis in the art for combining Yeo '815 and Shimizu to support a 35 U.S.C. §103(a) rejection of claim 1. Accordingly, for this mutually exclusive reason, the Examiner's burden of factually supporting a *prima facie* case of

obviousness cannot be met with respect to claim 1 and its dependent claims. Consequently, the rejection of claim 15 under 35 U.S.C. §103(a) is not applicable.

Claim 28

As described above, Yeo '815 fails to support a *prima facie* case of obviousness of claim 28 and its dependent claims. Moreover, Shimizu fails to correct the shortcomings of Yeo '815 because Shimizu also fails to teach an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; (2) a first gate interposing the first source/drain regions; and (3) first spacers on opposing sides of the first gate and each extending from the first gate to a first width; and wherein a second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; (2) a second gate interposing the second source/drain regions; and (3) second spacers on opposing sides of the second gate and each extending from the second gate to a second width, wherein the first and second widths are substantially different, where the substantial difference between the first and second widths at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first and second source/drain regions, respectively.

For example, Shimizu does not teach an NMOS device ***and*** a PMOS device ***each*** located partially over ***a*** substrate surface ***and*** isolated by an isolation region in the substrate. In addition, Shimizu also fails to teach that the NMOS and PMOS devices includes spacers extending from respective spacers to substantially different widths, where the substantial difference between the spacer widths at least indirectly causes a substantial difference in magnitudes of stresses in source/drain regions of the NMOS and PMOS devices. Consequently, rejections based on 35 U.S.C. §103(a) cannot be supported by the combination of Yeo '815 and Shimizu as applied to claim 28.

Therefore, it is impossible to render obvious the subject matter of claim 28 based on the combination of Yeo '815 and Shimizu, and the above explicit terms of the statute cannot be met. As a result, the Examiner's burden of factually supporting a *prima facie* case of obviousness

cannot be met with respect to claim 28 and its dependent claim 37, and a rejection under 35 U.S.C. §103(a) is not applicable.

There is still another compelling, and mutually exclusive, reason why the combination of Yeo '815 and Shimizu cannot be applied to reject claim 28 or its dependent claims under 35 U.S.C. §103(a). Here, the combination of Yeo '815 and Shimizu does not teach, or even suggest, the desirability of combination since neither Yeo '815 nor Shimizu teach or suggest an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; (2) a first gate interposing the first source/drain regions; and (3) first spacers on opposing sides of the first gate and each extending from the first gate to a first width; and wherein a second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; (2) a second gate interposing the second source/drain regions; and (3) second spacers on opposing sides of the second gate and each extending from the second gate to a second width, wherein the first and second widths are substantially different, where the substantial difference between the first and second widths at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first and second source/drain regions, respectively.

Thus, neither Yeo '815 nor Shimizu provide any incentive or motivation supporting the desirability of combination. Therefore, there is simply no basis in the art for combining Yeo '815 and Shimizu to support a 35 U.S.C. §103(a) rejection of claim 28 and its dependent claims. Accordingly, for this mutually exclusive reason, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 28 and its dependent claims. Consequently, the rejection of claim 37 under 35 U.S.C. §103(a) is not applicable.

Claim 38

As described above, Yeo '815 fails to teach any of the configurations recited in claim 38. Moreover, Shimizu fails to cure this shortcoming, because Shimizu also fails to teach an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of

the NMOS and PMOS devices includes one of: (1) first source/drain regions located at least partially within the substrate and comprising SiC; and (2) first source/drain regions located at least partially within the substrate and comprising SiGe; and wherein a second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions located at least partially within the substrate and comprising SiC wherein the first source/drain regions comprise SiGe; (2) second source/drain regions located at least partially within the substrate and comprising SiGe wherein the first source/drain regions comprise SiC; and (3) second source/drain regions located at least partially within the substrate and substantially not comprising either of SiC and SiGe.

Therefore, it is impossible to render obvious the subject matter of claim 38 based on the combination of Yeo '815 and Shimizu, and the above explicit terms of the statute cannot be met. As a result, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 38 and its dependent claim 43, and a rejection under 35 U.S.C. §103(a) is not applicable.

There is still another compelling, and mutually exclusive, reason why the combination of Yeo '815 and Shimizu cannot be applied to reject claim 38 under 35 U.S.C. §103(a). Here, the combination of Yeo '815 and Shimizu does not teach, or even suggest, the desirability of combination since neither teach or suggest an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions located at least partially within the substrate and comprising SiC; and (2) first source/drain regions located at least partially within the substrate and comprising SiGe; and wherein a second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions located at least partially within the substrate and comprising SiC wherein the first source/drain regions comprise SiGe; (2) second source/drain regions located at least partially within the substrate and comprising SiGe wherein the first source/drain regions comprise SiC; and (3) second source/drain regions located at least partially within the substrate and substantially not comprising either of SiC and SiGe.

Thus, neither Yeo '815 nor Shimizu provide any incentive or motivation supporting the desirability of combination. Therefore, there is simply no basis in the art for combining Yeo '815 and Shimizu to support a 35 U.S.C. §103(a) rejection of claim 38. Therefore, for this mutually exclusive reason, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 38 and its dependent claims. Consequently, the rejection of claim 43 under 35 U.S.C. §103(a) is not applicable.

**Rejections under 35 U.S.C. §103(a): Yeo '815 in view of Yeo '646**

Claims 8, 9, 32 and 33 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yeo '815 in view of Yeo '646. Applicants traverse these rejections on the grounds that the combination of Yeo '815 and Yeo '646 is defective in establishing a *prima facie* case of obviousness with respect to independent claims 1 and 28 and their dependent claims.

Claim 1

As described above, Yeo '815 fails to teach any of the configurations recited in claim 1. Moreover, Yeo '646 fails to cure this shortcoming, because Yeo '646 also fails to teach an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; and (2) a first gate interposing the first source/drain regions and having a first gate height over the surface; and wherein a second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; and (2) a second gate interposing the second source/drain regions and having a second gate height over the surface, wherein the first and second gate heights are substantially different, where the substantial difference between the first and second gate heights at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first and second source/drain regions, respectively. That is, Yeo '646 fails to teach any of the configurations recited in claim 1 in the manner described above with respect to Yeo '815.

Therefore, it is impossible to render obvious the subject matter of claim 1 based on the combination of Yeo '815 and Yeo '646, and the above explicit terms of the statute cannot be met. As a result, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 1, and a rejection under 35 U.S.C. §103(a) is not applicable to claim 1 or its dependent claims 8 and 9.

Another compelling and mutually exclusive reason why the combination of Yeo '815 and Yeo '646 cannot be combined and applied to reject claim 1 under 35 U.S.C. §103(a) is that the combination of Yeo '815 and Yeo '646 does not teach, or even suggest, the desirability of combination since neither Yeo '815 nor Yeo '646 teach or suggest providing an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; and (2) a first gate interposing the first source/drain regions and having a first gate height over the surface; and wherein a second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; and (2) a second gate interposing the second source/drain regions and having a second gate height over the surface, wherein the first and second gate heights are substantially different, where the substantial difference between the first and second gate heights at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first and second source/drain regions, respectively. That is, neither Yeo '815 nor Yeo '646 teach any of the configurations recited in claim 1 in the manner described above.

Thus, neither Yeo '815 nor Yeo '646 provide any incentive or motivation supporting the desirability of combination. Therefore, there is simply no basis in the art for combining Yeo '815 and Yeo '646 to support a 35 U.S.C. §103(a) rejection of claim 1. Accordingly, for this mutually exclusive reason, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 1 and its dependent claims. Consequently, the rejection of claims 8 and 9 under 35 U.S.C. §103(a) is not applicable.

Claim 28

As described above, Yeo '815 fails to support a *prima facie* case of obviousness of claim 28 and its dependent claims. Moreover, Yeo '646 fails to correct the shortcomings of Yeo '815 because Yeo '646 also fails to teach an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; (2) a first gate interposing the first source/drain regions; and (3) first spacers on opposing sides of the first gate and each extending from the first gate to a first width; and wherein a second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; (2) a second gate interposing the second source/drain regions; and (3) second spacers on opposing sides of the second gate and each extending from the second gate to a second width, wherein the first and second widths are substantially different, where the substantial difference between the first and second widths at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first and second source/drain regions, respectively.

For example, Yeo '646 does not teach an NMOS device ***and*** a PMOS device ***each*** located partially over ***a*** substrate surface ***and*** isolated by an isolation region in the substrate. In addition, Yeo '646 also fails to teach that the NMOS and PMOS devices includes spacers extending from respective spacers to substantially different widths, where the substantial difference between the spacer widths at least indirectly causes a substantial difference in magnitudes of stresses in source/drain regions of the NMOS and PMOS devices. Consequently, rejections based on 35 U.S.C. §103(a) cannot be supported by the combination of Yeo '815 and Yeo '646 as applied to claim 28.

Therefore, it is impossible to render obvious the subject matter of claim 28 based on the combination of Yeo '815 and Yeo '646, and the above explicit terms of the statute cannot be met. As a result, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 28 and it dependent claims 32 and 33, and a rejection under 35 U.S.C. §103(a) is not applicable.

There is still another compelling, and mutually exclusive, reason why the combination of Yeo '815 and Yeo '646 cannot be applied to reject claim 28 or its dependent claims under 35 U.S.C. §103(a). Here, the combination of Yeo '815 and Yeo '646 does not teach, or even suggest, the desirability of combination since neither Yeo '815 nor Yeo '646 teach or suggest an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; (2) a first gate interposing the first source/drain regions; and (3) first spacers on opposing sides of the first gate and each extending from the first gate to a first width; and wherein a second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; (2) a second gate interposing the second source/drain regions; and (3) second spacers on opposing sides of the second gate and each extending from the second gate to a second width, wherein the first and second widths are substantially different, where the substantial difference between the first and second widths at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first and second source/drain regions, respectively.

Thus, neither Yeo '815 nor Yeo '646 provide any incentive or motivation supporting the desirability of combination. Therefore, there is simply no basis in the art for combining Yeo '815 and Yeo '646 to support a 35 U.S.C. §103(a) rejection of claim 28 and its dependent claims. Accordingly, for this mutually exclusive reason, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 28 and its dependent claims. Consequently, the rejection of claims 32 and 33 under 35 U.S.C. §103(a) is not applicable.

**Rejections under 35 U.S.C. §103(a): Yeo '815 in view of Baba**

Claims 10, 34 and 35 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yeo '815 in view of Baba. Applicants traverse these rejections on the grounds that the combination of Yeo '815 and Baba is defective in establishing a *prima facie* case of obviousness with respect to independent claims 1 and 28 and their dependent claims.

Claim 1

As described above, Yeo '815 fails to teach any of the configurations recited in claim 1. Moreover, Baba fails to cure this shortcoming, because Baba also fails to teach an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; and (2) a first gate interposing the first source/drain regions and having a first gate height over the surface; and wherein a second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; and (2) a second gate interposing the second source/drain regions and having a second gate height over the surface, wherein the first and second gate heights are substantially different, where the substantial difference between the first and second gate heights at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first and second source/drain regions, respectively. That is, Baba fails to teach any of the configurations recited in claim 1 in the manner described above with respect to Yeo '815.

Therefore, it is impossible to render obvious the subject matter of claim 1 based on the combination of Yeo '815 and Baba, and the above explicit terms of the statute cannot be met. As a result, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 1, and a rejection under 35 U.S.C. §103(a) is not applicable to claim 1 or its dependent claim 10.

Another compelling and mutually exclusive reason why the combination of Yeo '815 and Baba cannot be combined and applied to reject claim 1 under 35 U.S.C. §103(a) is that the combination of Yeo '815 and Baba does not teach, or even suggest, the desirability of combination since neither Yeo '815 nor Baba teach or suggest providing an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; and (2) a first gate interposing the first source/drain regions and having a first gate height over the surface; and wherein a second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; and (2) a second gate

interposing the second source/drain regions and having a second gate height over the surface, wherein the first and second gate heights are substantially different, where the substantial difference between the first and second gate heights at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first and second source/drain regions, respectively. That is, neither Yeo '815 nor Baba teach any of the configurations recited in claim 1 in the manner described above.

Thus, neither Yeo '815 nor Baba provide any incentive or motivation supporting the desirability of combination. Therefore, there is simply no basis in the art for combining Yeo '815 and Baba to support a 35 U.S.C. §103(a) rejection of claim 1. Accordingly, for this mutually exclusive reason, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 1 and its dependent claims. Consequently, the rejection of claim 10 under 35 U.S.C. §103(a) is not applicable.

Claim 28

As described above, Yeo '815 fails to support a *prima facie* case of obviousness of claim 28 and its dependent claims. Moreover, Baba fails to correct the shortcomings of Yeo '815 because Baba also fails to teach an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; (2) a first gate interposing the first source/drain regions; and (3) first spacers on opposing sides of the first gate and each extending from the first gate to a first width; and wherein a second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; (2) a second gate interposing the second source/drain regions; and (3) second spacers on opposing sides of the second gate and each extending from the second gate to a second width, wherein the first and second widths are substantially different, where the substantial difference between the first and second widths at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first and second source/drain regions, respectively.

For example, Baba does not teach an NMOS device ***and*** a PMOS device ***each*** located partially over ***a*** substrate surface ***and*** isolated by an isolation region in the substrate. In addition, Baba also fails to teach that the NMOS and PMOS devices includes spacers extending from respective spacers to substantially different widths, where the substantial difference between the spacer widths at least indirectly causes a substantial difference in magnitudes of stresses in source/drain regions of the NMOS and PMOS devices. Consequently, rejections based on 35 U.S.C. §103(a) cannot be supported by the combination of Yeo '815 and Baba as applied to claim 28 or its dependent claims.

Therefore, it is impossible to render obvious the subject matter of claim 28 and its dependent claims based on the combination of Yeo '815 and Baba, and the above explicit terms of the statute cannot be met. As a result, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 28 and it dependent claims 34 and 35, and a rejection under 35 U.S.C. §103(a) is not applicable.

There is still another compelling, and mutually exclusive, reason why the combination of Yeo '815 and Baba cannot be applied to reject claim 28 or its dependent claims under 35 U.S.C. §103(a). Here, the combination of Yeo '815 and Baba does not teach, or even suggest, the desirability of combination since neither Yeo '815 nor Baba teach or suggest an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes: (1) first source/drain regions located at least partially in the substrate; (2) a first gate interposing the first source/drain regions; and (3) first spacers on opposing sides of the first gate and each extending from the first gate to a first width; and wherein a second one of the NMOS and PMOS devices includes: (1) second source/drain regions located at least partially in the substrate; (2) a second gate interposing the second source/drain regions; and (3) second spacers on opposing sides of the second gate and each extending from the second gate to a second width, wherein the first and second widths are substantially different, where the substantial difference between the first and second widths at least indirectly causes a substantial difference in magnitudes of first and second stresses in the first and second source/drain regions, respectively.

Thus, neither Yeo '815 nor Baba provide any incentive or motivation supporting the desirability of combination. Therefore, there is simply no basis in the art for combining Yeo '815 and Baba to support a 35 U.S.C. §103(a) rejection of claim 28 and its dependent claims. Accordingly, for this mutually exclusive reason, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 28 and its dependent claims. Consequently, the rejection of claims 34 and 35 under 35 U.S.C. §103(a) is not applicable.

**Rejections under 35 U.S.C. §103(a): Yeo '815 in view of Wu**

Claim 39 was rejected under 35 U.S.C. §103(a) as being unpatentable over Yeo '815 in view of U.S. Patent No. 6,348,390 to Wu ("Wu"). Applicants traverse this rejection on the grounds that the combination of Yeo '815 and Wu is defective in establishing a *prima facie* case of obviousness with respect to independent claim 38 and its dependent claims.

Claim 38

As described above, Yeo '815 fails to teach any of the configurations recited in claim 38. Moreover, Wu fails to cure this shortcoming, because Wu also fails to teach an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions located at least partially within the substrate and comprising SiC; and (2) first source/drain regions located at least partially within the substrate and comprising SiGe; and wherein a second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions located at least partially within the substrate and comprising SiC wherein the first source/drain regions comprise SiGe; (2) second source/drain regions located at least partially within the substrate and comprising SiGe wherein the first source/drain regions comprise SiC; and (3) second source/drain regions located at least partially within the substrate and substantially not comprising either of SiC and SiGe.

Therefore, it is impossible to render obvious the subject matter of claim 38 based on the combination of Yeo '815 and Wu, and the above explicit terms of the statute cannot be met. As a result, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot

be met with respect to claim 38, and a rejection under 35 U.S.C. §103(a) is not applicable to claim 38 or its dependent claim 39.

There is still another compelling, and mutually exclusive, reason why the combination of Yeo '815 and Wu cannot be applied to reject claim 38 under 35 U.S.C. §103(a). Here, the combination of Yeo '815 and Wu does not teach, or even suggest, the desirability of combination since neither teach or suggest an NMOS device and a PMOS device each located partially over a substrate surface, wherein a first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions located at least partially within the substrate and comprising SiC; and (2) first source/drain regions located at least partially within the substrate and comprising SiGe; and wherein a second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions located at least partially within the substrate and comprising SiC wherein the first source/drain regions comprise SiGe; (2) second source/drain regions located at least partially within the substrate and comprising SiGe wherein the first source/drain regions comprise SiC; and (3) second source/drain regions located at least partially within the substrate and substantially not comprising either of SiC and SiGe.

Thus, neither Yeo '815 nor Wu provide any incentive or motivation supporting the desirability of combination. Therefore, there is simply no basis in the art for combining Yeo '815 and Wu to support a 35 U.S.C. §103(a) rejection of claim 38. Accordingly, for this mutually exclusive reason, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 38 and its dependent claims. Consequently, the rejection of claim 39 under 35 U.S.C. §103(a) is not applicable.

**Rejections under 35 U.S.C. §103(a): Rodder in view of Wu**

Claims 47-49 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,187,641 to Rodder, et al. ("Rodder") in view of Wu. Applicants traverse these rejections on the grounds that the combination of Rodder and Wu is defective in establishing a *prima facie* case of obviousness with respect to independent claim 47 and its dependent claims.

Claim 47

Claim 47 recites:

> 47. An integrated circuit device, comprising:
> a plurality of semiconductor devices each including:
> an isolation region located in a substrate;
> an NMOS device located partially over a surface of the substrate; and
> a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface;
> wherein, in ones of the plurality of semiconductor devices, a first one of the NMOS and PMOS devices includes one of:
> first source/drain regions recessed within the surface; and
> first source/drain regions extending from the surface; and
> wherein, in ones of the plurality of semiconductor devices, a second one of the NMOS and PMOS devices includes one of:
> second source/drain regions recessed within the surface wherein the first source/drain regions extend from the surface;
> second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and
> second source/drain regions substantially coplanar with the surface; and
> a plurality of interconnects connecting ones of the plurality of semiconductor devices.

To support a rejection with respect to claim 47, the combination of Rodder and Wu must contain all of the elements of claim 47. However, the combination of Rodder and Wu fails to teach an NMOS device and a PMOS device each located partially over a substrate surface and isolated by an isolation region in the substrate, wherein a first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions recessed within the surface, and (2) first source/drain regions extending from the surface; and wherein a second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions recessed within the surface

wherein the first source/drain regions extend from the surface; (2) second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and (3) second source/drain regions substantially coplanar with the surface.

For example, to support a rejection of claim 47, the combination of Rodder and Wu must teach an NMOS device and a PMOS device each located partially over a substrate surface and isolated by an isolation region in the substrate, but neither Rodder nor Wu teach an NMOS device ***and*** a PMOS device ***each*** located partially over ***a*** substrate surface ***and*** isolated by an isolation region in the substrate. In contrast, Rodder and Wu only explicitly disclose a single MOS device.

In addition, to support a rejection of claim 47, the combination of Rodder and Wu must also teach that one of an NMOS device and a PMOS device includes first source/drain regions that are either recessed within or extending from the substrate surface, and that the other of the NMOS device and the PMOS device includes second source/drain regions that are:

- recessed within the substrate surface if the first source/drain regions extend from the substrate surface;
- extending from the substrate surface if the first source/drain regions are recessed within the substrate surface; or
- substantially coplanar with the substrate surface.

Thus, to support a rejection of claim 47, the combination of Rodder and Wu must teach an NMOS device ***and*** a PMOS device ***each*** located partially over ***a*** substrate surface ***and*** isolated by an isolation region in the substrate where:

- the NMOS device includes source/drain regions that are recessed within the substrate surface, and the PMOS device includes source/drain regions that are extending from the substrate surface;

- the PMOS device includes source/drain regions that are recessed within the substrate surface, and the NMOS device includes source/drain regions that are extending from the substrate surface;
- the NMOS device includes source/drain regions that are recessed within the substrate surface, and the PMOS device includes source/drain regions that are substantially coplanar with the substrate surface;
- the PMOS device includes source/drain regions that are recessed within the substrate surface, and the NMOS device includes source/drain regions that are substantially coplanar with the substrate surface;
- the NMOS device includes source/drain regions that are extending from the substrate surface, and the PMOS device includes source/drain regions that are substantially coplanar with the substrate surface; or
- the PMOS device includes source/drain regions that are extending from the substrate surface, and the NMOS device includes source/drain regions that are substantially coplanar with the substrate surface.

However, the combination of Rodder and Wu fails to teach any of these configurations. Consequently, rejections based on 35 U.S.C. §103(a) cannot be supported by the combination of Rodder and Wu as applied to claim 47. Therefore, it is impossible to render obvious the subject matter of claim 47 based on the combination of Rodder and Wu, and the above explicit terms of the statute cannot be met. As a result, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 47, and a rejection under 35 U.S.C. §103(a) is not applicable to claim 47 or its dependent claims.

There is still another compelling, and mutually exclusive, reason why the combination of Rodder and Wu cannot be combined and applied to reject claim 47 under 35 U.S.C. §103(a). That is, the combination of Rodder and Wu does not teach, or even suggest, the desirability of combination since neither Rodder nor Wu teach or suggest an NMOS device and a PMOS device each located partially over a substrate surface and isolated by an isolation region in the substrate,

wherein a first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions recessed within the surface, and (2) first source/drain regions extending from the surface; and wherein a second one of the NMOS and PMOS devices includes one of: (1) second source/drain regions recessed within the surface wherein the first source/drain regions extend from the surface; (2) second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and (3) second source/drain regions substantially coplanar with the surface. That is, neither Rodder nor Wu teach or suggest any of the configurations recited in claim 47 in the manner described above.

Thus, neither Rodder nor Wu provide any incentive or motivation supporting the desirability of combination. Therefore, there is simply no basis in the art for combining Rodder and Wu to support a 35 U.S.C. §103(a) rejection of claim 47. Therefore, for this mutually exclusive reason, the Examiner's burden of factually supporting a *prima facie* case of obviousness cannot be met with respect to claim 47 and its dependent claims. Consequently, the rejection of claims 47-49 under 35 U.S.C. §103(a) is not applicable.

**Conclusion**

It is clear from the foregoing that independent claims 1, 16, 28, 38, 44 and 47 are in condition for allowance. Dependent claims 2-15, 17-27, 29-37, 39-43, 45, 46, 48 and 49 depend from and further limit independent claims 1, 16, 28, 38, 44 and 47, in a patentable sense. Therefore, claims 2-15, 17-27, 29-37, 39-43, 45, 46, 48 and 49 are also in condition for allowance.

Consequently, an early formal notice of allowance of claims 1-49 is requested.

Respectfully submitted,

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